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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/700,874	01/02/2001	Kazuhisa Fujimoto	501.39293X00	8035

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EXAMINER
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ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 12/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/700,874	Applicant(s) FUJIMOTO ET AL.	
	Examiner Kimberly N. McLean-Mayo	Art Unit 2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,18-31,36-39,41 and 42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-16,18-31,36-39,41 and 42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The enclosed detailed action is in response to the Application submitted on January 2, 2001.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

4. Figures 2 and 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Oath/Declaration

5. The Oath/Declaration is defective because it does not provide a claim for domestic priority under 35 U.S.C. 120.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-16, 18-31, 36-39 and 41-42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claims 1-12, it is not clear from the specification or the claims what the Applicant means by package.

With respect to claims 6-7, 13-16, 18-31, 36-39 and 41-42, it is not clear from the specification or the claims what the Applicant means by platter.

8. Claim 22 and 38, Line 4 states, "storing control data for the disk drives are mounted". It is not clear what this limitation means.

9. Claim 25 recites the limitation "the platter" in Lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 1-15, 18-20, 22-31, 37 and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Brant et al. (USPN: 5,887,270).

Regarding claims 1, 6-7 and 30, Brant discloses a disk array controller comprising a channel interface package in which at least a channel unit (internal logic which interfaces with the host computer) with a host computer and an access path interface unit (internal logic which interfaces with external elements) are packaged (Figure 3, Reference 11); a disk interface package in which at least a disk interface with a disk drive and an access path interface unit are packaged (Figure 3, References 25, 27, 29, 31); and a memory package in which a memory unit for storing control data for the disk drive and an access path interface unit (internal logic which interfaces with external logic) are packaged (Figure 3, References 12 and 20), and that connections are made between the access path interface unit in the channel interface package and the access path interface unit in the memory package (Figure 3 shows 18A coupling the channel interface package to the memory package thereby coupling the internal elements of both packages) and between the access path interface unit in the disk interface package and the access path interface unit in the memory package by cables (Figure 3 shows 18A coupling the disk interface package to the memory package thereby coupling the internal elements of both packages).

Regarding claim 2, Brant discloses the disk array controller comprising plural memory packages, wherein connections are made between the access path interface unit in the channel interface package an the access path interface unit in each of the plural memory packages by cables (Figure 1 and 3, References 12/20 and 13/21).

Regarding claim 3, Brant discloses the plural memory packages interconnected by cables (Figures 1 and 3, signal means coupling references 12 and 13).

Regarding claim 4, Brant discloses that the memory units packaged in the plural memory packages store the same data (C 5, L 58-67; C 6, L 1-3).

Regarding claim 5, Brant discloses that power is supplied from different power supplies to the plural memory packages (Figure 3, References 46 and 50; C 7, L 20-42).

Regarding claim 8, Brant discloses a disk array controller comprising a channel interface package in which at least a channel unit with a host computer and an access path interface unit are packaged (Figure 3, Reference 11); a disk interface package in which at least a disk interface with a disk drive and an access path interface unit are packaged (Figure 3, References 25, 27, 29, 31); and a cache memory package in which a cache memory unit for temporarily storing data to be recorded into the disk drive and an access path interface unit are packaged (Figure 3, References 12 and 20), and that connections are made between the access path interface unit in

the channel interface package and the access path interface unit in the cache memory package (Figure 3 shows 18A coupling the channel interface package to the cache memory package thereby coupling the internal elements of both packages) and between the access path interface unit in the disk interface package and the access path interface unit in the cache memory package by cables (Figure 3 shows 18A coupling the disk interface package to the memory package thereby coupling the internal elements of both packages).

Regarding claim 9, Brant discloses the disk array controller comprising plural cache memory packages, wherein connections are made between the access path interface unit in the channel interface package and the access path interface unit in each of the plural cache memory packages by cables (Figure 1 and 3, References 12/20 and 13/21).

Regarding claim 10, Brant discloses the plural cache memory packages interconnected by cables (Figures 1 and 3, signal means coupling references 12 and 13).

Regarding claim 11, Brant discloses that the cache memory units mounted in the plural cache memory packages store the same data (C 5, L 58-67; C 6, L 1-23).

Regarding claim 12, Brant discloses that power is supplied from different power supplies to the plural cache memory packages (Figure 3, References 46 and 50; C 7, L 20-42).

Regarding claims 13-14, Brant discloses a disk array controller comprising an interface platter on which a channel interface unit to be connected with a host computer and a disk interface unit to be connected with a disk drive are mounted (Figures 1 and 3, Reference 11); a memory platter on which a memory unit for storing control data for the disk drive is mounted (Figures 1 and 3, References 12 and 20); a cable which connects the interface platter and the memory platter (Figures 1 and 3, Reference 18); and a selector unit, connected with the channel interface unit, the disk interface unit and the memory unit, which selects requests from the channel interface and the disk interface unit (Figures 1 and 3, Reference 17; C 5, L 28-32).

Regarding claim 15, Brant discloses the selector unit and the memory unit are connected (Figures 1 and 3 show Reference 17 coupled to References 12/20 via Reference 18)

Regarding claims 18-19, Brant discloses a disk array controller comprising an interface platter on which a channel interface unit to be connected with a host computer and a disk interface unit to be connected with a disk drive are mounted (Figures 1 and 3, Reference 11); a memory platter on which a cache memory unit for storing data to be recorded into the disk drive is mounted (Figures 1 and 3, References 12 and 20); a cable which connects the interface platter and the memory platter (Figures 1 and 3, Reference 18); and a selector unit, connected with the channel interface unit, the disk interface unit and the memory unit, which selects requests from the channel interface and the disk interface unit (Figures 1 and 3, Reference 17; C 5, L 28-32).

Regarding claim 20, Brant discloses the selector unit and the cache memory unit are connected (Figures 1 and 3 show Reference 17 coupled to References 12/20 via Reference 18)

Regarding claims 22-23, Brant discloses a disk array controller (Figure 4) comprising plural platters on each of which a channel interface unit to be connected with a host computer, a disk interface to be connected with a disk drive and a memory unit for storing control data for the disk drive are mounted (Figure 4, References 60 and 70); a cable which interconnects the plural platters (Figure 4, Reference 22).

Regarding claims 24-26, Brant discloses a selector unit, connected with the channel interface unit, the disk interface unit and the memory unit which are mounted on one of the plural platters, which selects requests from the channel interface and the disk interface unit (Figures 1 and 3, Reference 17; C 5, L 28-32).

Regarding claims 27-29, Brant discloses a disk array controller (Figure 4) comprising plural platters on each of which a channel interface unit to be connected with a host computer, a disk interface to be connected with a disk drive and a cache memory unit for storing control data for the disk drive are mounted (Figure 4, References 60 and 70); a cable which interconnects the plural platters (Figure 4, Reference 22); a selector unit, connected with the channel interface unit, the disk interface unit and the cache memory unit, which selects requests from the channel

interface and the disk interface unit (the selector unit, shown in Figures 1 and 3, Reference 17; C 5, L 28-32, in References 60 and 70 of Figure 4).

Regarding claim 31, Brant discloses a fourth platter on which a cache memory unit for storing data to be recorded into the disk drive is mounted (Figures 1 and 3, References 13 and 21); a cable which connects the first and fourth platters (Figures 1 and 3 show References 13/21 coupled to Reference 11A via Reference 18); and a cable which connects the second and fourth platters (Figures 1 and 3 show References 13/21 coupled to References 25, 27, 29 and 31 via Reference 18).

Regarding claim 37, a disk array controller comprising plural interface platters on each of which a channel interface unit to be connected with a host computer and a disk interface unit to be connected with a disk drive are mounted (Figures 1 and 3, References 11A and 11B); and a memory platter on which a memory unit for storing control data for the disk drive is mounted, wherein the memory platter is located between the plural interface platters (Figures 1 and 3, References 12 and 20).

Regarding claim 42, a disk array controller comprising plural interface platters on each of which a channel interface unit to be connected with a host computer and a disk interface unit to be connected with a disk drive are mounted (Figures 1 and 3, References 11A and 11B); and a memory platter on which a cache memory unit for storing control data for the disk drive is

mounted, wherein the memory platter is located between the plural interface platters (Figures 1 and 3, References 12 and 20).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 16, 21, 36, 38-39 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brant (USPN: 5,887,270).

Regarding claims 16 and 21, Brant discloses the limitations cited above in claims 13 and 18, however, Brant does not explicitly disclose the selector unit mounted on the reverse of the surface on which the channel interface unit and the disk interface unit are mounted. However, it is well known in the art to mount elements on both sides of a surface to conserve space and minimize the size of the surface. Hence it would have been obvious to one of ordinary skill in the art to store the selector unit on the reverse of the surface on which the channel interface unit and the disk interface unit are mounted for the desirable purpose of conserving space and size minimization.

Regarding claim 36, Brant discloses an interface platter on which a channel interface unit to be connected with a host computer and a disk interface unit to be connected with a disk drive are mounted (Figures 1 and 3, Reference 11); and a memory platter on which a memory unit for

storing control data for the disk drive is mounted (Figures 1 and 3, References 12 and 20). Brant dose not explicitly disclose that the interface platter is perpendicular to the memory platter. However, it is known in the art that the lay out process for elements on a substrate are implemented to obtain certain goals based such as space requirements, timing parameters, delays, etc. Hence, it would have been obvious to locate the interface platter perpendicular to the memory platter in Brant's system to obtain specific design goals.

Regarding claims 38-39, Brant discloses a disk array controller (Figure 4) comprising plural platters on each of which a channel interface unit to be connected with a host computer, a disk interface to be connected with a disk drive and a memory unit for storing control data for the disk drive are mounted (Figure 4, References 60 and 70); a cable which interconnects the plural platters (Figure 4, Reference 22). Brant does not disclose one of the platters located above another one of the plural platters (vertically). However, it is known in the art that the lay out process for elements on a substrate are implemented to obtain certain goals based such as space requirements, timing parameters, delays, etc. Hence, it would have been obvious to locate the one of the plural platters vertical to another one of the plural platters in Brant's system for the desirable purpose of obtaining specific design goals.

Regarding claim 41, Brant discloses an interface platter on which a channel interface unit to be connected with a host computer and a disk interface unit to be connected with a disk drive are mounted (Figures 1 and 3, Reference 11); and a memory platter on which a cache memory unit

for storing data to be recorded into the disk drive is mounted (Figures 1 and 3, Reference 12 and 20). Brant does not explicitly disclose that the interface platter is perpendicular to the memory platter. However, it is known in the art that the lay out process for elements on a substrate are implemented to obtain certain goals based such as space requirements, timing parameters, delays, etc. Hence, it would have been obvious to locate the interface platter perpendicular to the memory platter in Brant's system to obtain specific design goals.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fujimoto et al. – USPN: 6,477,619 – interconnected cables for connected units in a disk array.

Gold et al. – USPN: 6,006,296 – scalable memory controller.

Chisholm et al. – USPN: 6,115,764 – redundant path access.

Fujimoto – USPN: 6,385,681 - interconnected cables for connected units in a disk array.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo can be reached on 703-308-4908. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-746-7329 for regular communications and 703-746-7240 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

November 26, 2002